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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known see 37 C.F.R. 1.5) 09/806136
INTERNATIONAL APPLICATION NO. PCT/JP00/05055	INTERNATIONAL FILING DATE 28 JULY 2000	PRIORITY DATE CLAIMED 28 JULY 1999

TITLE OF INVENTION **RECORDING SYSTEM, DATA RECORDING APPARATUS, MEMORY APPARATUS, AND DATA RECORDING METHOD**

APPLICANT(S) FOR DO/EO/US **Kenichi NAKANISHI and Shigeo ARAKI**

Applicants herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. ☐ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 – 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information:

    PCT/RO/101, PCT/ISA/210
    15 Sheets of Drawings

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U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/806136	INTERNATIONAL APPLICATION NO. PCT/JP00/05055	ATTORNEY'S DOCKET NO. 450106-02621

21. ☒ The following fees are submitted	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5): Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO .. ..$1000.00 International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO .....$860.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO .....$710.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)...$690.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4).....$100.00		
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CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	6 - 20 =	0	x $18.00	$ 0.00	
Independent Claims	4 - 3 =	1	x $80.00	$ 80.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$	
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SEND ALL CORRESPONDENCE TO:

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Dated: March 26, 2001

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34,930
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Nakanishi et al.
Serial No.:	To be assigned
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Title of Invention:	RECORDING SYSTEM, DATA RECORDING APPARATUS, MEMORY APPARATUS, AND DATA RECORDING METHOD

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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Box Patent Application (35 U.S.C. 111)
Washington, D.C. 20231

Sir:

Before the issuance of the first Office Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claim 4 as follows:

4. (Amended) An apparatus according to claim 1, wherein

an access is performed with reference to a logic cluster address/physical cluster address converstion table.

REMARKS

Claims 1-6 remain in the application. Claim 4 has been amended to eliminate multiple dependencies. Attached hereto is a marked up version of the changes made to claim 4 by the current amendment. The attached page is captioned **"Version with markings to show changes made."** The filing fee has been calculated based upon these amendments to the claims.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

4. (Amended) An apparatus according to claim 1 ~~2, or 3~~, wherein

an access is performed with reference to a logic cluster address/physical cluster address converstion table.

DESCRIPTION

RECORDING SYSTEM, DATA RECORDING APPARATUS, MEMORY APPARATUS, AND DATA RECORDING METHOD

Technical Field

The invention relates to a recording system, a data recording apparatus, a memory apparatus, and a data recording method, in which a memory card which is detachable to/from an apparatus is used as a recording medium.

Background Art

According to an electrically rewritable non-volatile memory called EEPROM (Electrically Erasable Programmable ROM), since one bit is constructed by two transistors, an occupation area per bit is large and there is a limitation in case of raising an integration degree. To solve such a problem, a flash memory in which one bit can be realized by one transistor by an all-bit batch erasing method has been developed. The flash memory is expected as a memory which can be substituted for a recording medium such as magnetic disk, optical disk, or the like.

It is known that a memory card having a flash memory is constructed so as to be detachable to/from an apparatus. By using such a memory card, a digital audio recording and reproducing apparatus using the memory card in place of the conventional

disk-shaped medium such as CD (Compact Disc), MD (Minidisc), or the like can be realized. Besides audio data, still image data and motion image data can be also recorded into the memory card and it can be used as a recording medium of a digital still camera or a digital video camera.

According to the flash memory, a data unit called a segment is divided into a predetermined number of clusters (fixed length) and one cluster is divided into a predetermined number of sectors (fixed length). The cluster is also called a block. The sector is also called a page. In the flash memory, an erasure is performed in a lump on a cluster unit basis, and the writing or reading operation is performed in a lump on a sector unit basis.

For example, in case of the flash memory of 4 MB (megabytes), as shown in Fig. 12, one segment is divided into 512 clusters. The segment is a unit for managing a predetermined number of clusters. One cluster is divided into 16 sectors. One cluster has a capacity of 8 kB (kbytes). One sector has a capacity of 512 B. A memory of a capacity of 16 MB can be constructed by using four segments each having a capacity of 4 MB.

As shown in Fig. 13A, logic cluster addresses are allocated to a memory space of 16 MB.

The logic cluster address is set to a length of 2 bytes in order to distinguish 512 × 4 = 2048 clusters. In Fig. 13A, the logic cluster address is expressed by a hexadecimal number. 0x denotes the hexadecimal notation. A logic address is an address which is logically handled by a data processing apparatus (software). A physical address is added to each cluster in the flash memory. A correspondence relation between the clusters and the physical addresses is unchanged.

According to the flash memory, by rewriting data, an insulating film deteriorates and the number of rewriting times is limited. Therefore, it is necessary to prevent a situation such that accesses are repetitively and concentratedly performed to a certain same memory area (cluster). Therefore, in case of rewriting data in a certain logic address stored in a certain physical address, in a file system of the flash memory, updated data is not rewritten to an unused cluster. Thus, the correspondence relation between the logic addresses and the physical addresses before the data updating changes after the updating. By performing such a swapping process as mentioned above, the situation such that the accesses are repetitively and concentratedly performed to the same cluster is prevented, so that a life of the flash memory can be

extended.

Since the logic cluster address is accompanied by the data which has once been written into the cluster, even if physical cluster addresses in which the data before updating and the data after the updating are written are changed, the same address is seen from a file management system and the subsequent accesses can be properly performed. Since the correspondence relation between the logic addresses and the physical addresses is changed by the swapping process, a logical/physical address conversion table showing the correspondence between them is needed. By referring to such a table, the physical cluster address corresponding to the designated logic cluster address is specified, thereby enabling the access to the cluster shown by the specified physical cluster address to be performed.

The logical/physical address conversion table is stored in a memory by the data processing apparatus. If a memory capacity of the data processing apparatus is small, the table can be stored in the flash memory. Fig. 13B shows an example of a logical/physical address conversion table regarding segment 1. As shown in Fig. 13B, in the logical/physical address conversion table, the physical cluster addresses (2 bytes) are made to

correspond to the logic cluster addresses (2 bytes) arranged in the ascending order, respectively. The logical/physical address conversion table is managed every segment and its size increases in accordance with the capacity of the flash memory.

There is a case where it is desirable to set a data writing speed to be higher than the ordinary one by making a plurality of storages of the flash memory operative in parallel. For example, an electronic music distribution EMD for distributing music data through a network is being put into practical use. The distributed music data is stored into a hard disk of a personal computer, data of a desired music piece is copied or moved into a memory card by the personal computer, and the memory card is attached into a portable recorder, so that the user can easily listen to the desired music at a place other than his home. Data of a plurality of music pieces is downloaded into the memory card from the hard disk by a parallel writing operation (at a high speed) and, upon reproduction, the music data is read out from the memory card at a normal speed.

Fig. 14 shows a construction of a conventional logic address for four storages. In the example of the diagram, address spaces in the memory are expressed by 11 bits of A0, A1, …, and

A10. A0 denotes the LSB (least significant bit) and A10 indicates the MSB (most significant bit). The storages each having a capacity of 4 MB are switched by the MSB (A10) and the second MSB (A9). Addresses of 9 bits of A0 to A8 are allocated to a sector and a segment in each storage.

When data is written, the operation is executed at a timing as shown in Fig. 15. First, the data is transferred from the host side to a page buffer of a sector size. Time T is required to transfer. In a next write busy period, the data is transferred from the page buffer into a flash buffer in the flash memory and the data is written into the storage.

Upon reading, as shown in Fig. 16, the data is read out from the flash memory for a read busy period. The read-out data is transferred to a page buffer of a sector size. In the next transfer time T, the data is transferred from the page buffer to the host side.

Fig. 17 is a flowchart showing a flow of processes in case of writing data into continuous logic sectors 0 to 3 belonging to different clusters in a certain segment. In first step S11, a logical/physical conversion table is formed with respect to a segment as a target to be written. In step S12, sector 0 is sent from the host side. The

time T is required for this transfer. In step S13, sector 0 is written into the flash memory. In step S14, sector 1 is sent from the host side. In step S15, sector 1 is written into the flash memory. Processes for sending of sector 2 (step S16), writing of sector 2 (step S17), sending of sector 3 (step S18), and writing of sector 3 (step S19) are sequentially performed. Hitherto, for example, even if four storages are provided in parallel, since accesses are concentrated to one storage, a high processing speed cannot be realized.

As for a data construction of one sector on the flash memory, as shown in Fig. 18, an area having a length of 16 bytes in which management information is recorded is added to data of 512 bytes. The management information comprises a logic cluster number, cluster management information, and attribute information. The cluster management information is set to the same information among all sectors in a certain cluster and includes information indicative of "valid/invalid" of the cluster or the like. The attribute information is information of every sector and includes copyright information or the like. For example, when the flash memory is attached into the apparatus, the host side reads the management information and forms a table of the logic cluster and the physical

cluster with respect to the segment.

In case of making a plurality of storages operative in parallel, it is necessary to consider a method of accessing to a plurality of storages. Fig. 19 shows a construction of supplying addresses to four storages. Fig. 20 shows addresses in a flash memory of 4 MB × 4 = 16 MB. As described with reference to Fig. 14, the addresses are expressed by 11 bits of A0, A1, …, and A10. A0 is the LSB (least significant bit) and A10 is the MSB (most significant bit). The storages each having a capacity of 4 MB are switched by the MSB (A10) and the second MSB (A9). The addresses of 9 bits of A0 to A8 are allocated to the clusters in each storage.

Hitherto, to switch the four storages, the addresses are supplied to the flash memory as shown in Fig. 19. The addresses A0 to A8 of 9 bits on the lower side are allocated in common to the four storages (0 to 3). The addresses A9 and A10 of 2 bits on the upper side are supplied to a 2-to-4 decoder 60. Selection signals CS0, CS1, CS2, and CS3 for selecting the storages are generated from the decoder 60.

In case of (A10, A9) = 00, the selection signal CS0 to select the storage 0 is generated from the decoder 60. When (A10, A9) = 01, (A10, A9) = 10, or (A10, A9) = 11, each of the selection signals CS1,

CS2, and CS3 for selecting each of the storage 1, storage 2, and storage 3 is generated from the decoder 60.

An address change at the time when the address is increased from a state where all of 11 bits are equal to 0 to a state where they are equal to 1 due to the switching of the storages as mentioned above is shown by arrows in Fig. 20. That is, when the address changes from the head cluster of the storage 0 to the final cluster of the storage 0, the cluster address changes so as to subsequently shift to the head cluster of the storage 1. Fig. 21 shows an arrangement of the segments and the logic cluster addresses.

In the conventional switching of the storages of the flash memory mentioned above, a storage selection signal is formed by using a few bits from the MSB of the address. Thus, the segments are concentratedly arranged onto one storage and the segments are different every storage. According to such a method, a plurality of clusters of the same segment cannot be simultaneously written in parallel. For example, since four clusters (0x0004, 0x0005, 0x0006, 0x0007) in Fig. 21 are included in the same storage 0, they cannot be simultaneously written.

The clusters of a plurality of segments,

for example, four clusters (0x0004, 0x0204, 0x0404, 0x0604) in Fig. 21 can be simultaneously written into the storages 0 to 3. However, according to the flash memory, since a logical/physical address conversion table is constructed every segment, it is necessary to refer to the logical/physical address conversion table upon accessing. Therefore, like an example mentioned above, when four clusters are simultaneously written over four segments, a memory for holding address conversion tables of four segments is needed. Each time the data of one sector is written into each segment, the necessity of referring to the address conversion table is caused. Performance upon writing (or upon reading) is deteriorated due to an overhead which is caused there.

It is, therefore, an object of the invention to provide a data processing system, a data processing apparatus, a memory apparatus, and a data recording method, in which data can be written in parallel into a plurality of storages and performance upon reading can be improved.

Disclosure of Invention

To solve the above problems, according to the invention of Claim 1, there is provided a data processing system in which a non-volatile memory apparatus having a plurality of storages in which

one cluster is constructed by a plurality of sectors and one segment is constructed by a plurality of clusters is detachable to/from a data processing apparatus, wherein

the data processing apparatus has

address designating means for designating an address of the cluster in which data is recorded,

the memory apparatus has

recording means for recording the data into the address designated by the address designating means, and

the data of a plurality of clusters in one segment is distributed and arranged into a plurality of storages.

According to the invention of Claim 2, there is provided a data processing apparatus using a non-volatile memory apparatus, as a recording medium, having a plurality of storages in which one cluster is constructed by a plurality of sectors and one segment is constructed by a plurality of clusters, wherein

data of a plurality of clusters in one segment is written into the memory apparatus so as to be distributed and arranged into a plurality of storages.

According to the invention of Claim 3, there is provided a non-volatile memory apparatus

which is detachable to/from a data processing apparatus and has a plurality of storages in which one cluster is constructed by a plurality of sectors and one segment is constructed by a plurality of clusters, wherein

data of the plurality of clusters in one segment is distributed and arranged into a plurality of storages.

According to the invention of Claim 6, there is provided a data recording method of recording, in parallel, data in which one cluster is constructed by a plurality of sectors and which exists over a plurality of clusters into a plurality of storages, comprising the steps of:

designating a cluster address and writing data into the designated cluster address; and

after completion of the parallel writing process, distributing and arranging the data of a plurality of clusters in one segment into a plurality of storages.

According to the invention, the data of a plurality of clusters in one segment can be written in parallel. When the written data is read out, if the data exists in the same segment, the switching of the logical/physical address conversion table is not caused, so that the performance upon reading can be improved.

Brief Description of Drawings

Fig. 1 is a block diagram showing a whole construction of an embodiment of the invention;

Fig. 2 is a block diagram schematically showing a construction of a memory card in the embodiment of the invention;

Fig. 3 is a block diagram showing a more detailed construction of the memory card in the embodiment of the invention;

Fig. 4 is a schematic diagram for explaining an address construction in the embodiment of the invention;

Fig. 5 is a schematic diagram for explaining the parallel writing operation in the embodiment of the invention;

Fig. 6 is a timing chart for explaining the writing operation in the embodiment of the invention;

Fig. 7 is a timing chart for explaining the reading operation in the embodiment of the invention;

Fig. 8 is a flowchart for explaining the writing operation in the embodiment of the invention;

Fig. 9 is a block diagram for explaining the switching of storages in the embodiment of the invention;

Fig. 10 is a schematic diagram for explaining the switching of storages in the embodiment of the invention;

Fig. 11 is a schematic diagram showing the relation between segments and logic cluster addresses in the embodiment of the invention;

Fig. 12 is a schematic diagram showing a construction of an example of a flash memory to which the invention can be applied;

Fig. 13 is a schematic diagram showing an example of a logical/physical address conversion table of the flash memory to which the invention can be applied;

Fig. 14 is a schematic diagram for explaining a conventional address construction;

Fig. 15 is a timing chart for explaining the conventional writing operation;

Fig. 16 is a timing chart for explaining the conventional reading operation;

Fig. 17 is a flowchart for explaining the conventional writing operation;

Fig. 18 is a schematic diagram for explaining a sector construction and management information;

Fig. 19 is a block diagram for explaining the conventional switching of storages;

Fig. 20 is a schematic diagram for

explaining the conventional switching of storages; and

Fig. 21 is a schematic diagram showing the conventional relation between segments and logic cluster addresses.

Best Mode for Carrying Out the Invention

An embodiment of the invention will now be described hereinbelow. Fig. 1 shows a construction of a system to which the invention can be applied. In the system, a data processing apparatus on the host side and a memory card are connected via a serial interface. In Fig. 1, reference numeral 1 denotes a CPU. A memory 2, a display 3, and an input/output unit 4 are connected to a bus of the CPU 1.

A serial interface 5 is arranged between the CPU bus and a memory card 6 surrounded by a broken line. The memory 2 includes an ROM for storing a program and an RAM which is used as a work area. Specifically speaking, the data processing apparatus is a personal computer, a digital still camera, a digital video camera, a digital audio recorder, or the like. The memory card 6 has a flash memory 7. The flash memory 7 is, for example, an NAND-type flash memory (non-volatile memory). There is also a case where an enciphering circuit is assembled in the memory card 6 for the purpose of

protection of the copyright of contents which are stored.

The invention can be also applied to a case where the transmission and reception of data between the data processing apparatus and the memory card 6 are executed by a parallel interface instead of the serial interface.

The flash memory 7 is a memory having a capacity of, for example, 4 MB × 4 = 16 MB. As mentioned with reference to Fig. 12, in case of the flash memory of 4 MB (megabytes), one segment is divided into 512 clusters and one cluster is divided into 16 sectors. One cluster has a capacity of 8 kB (kbytes) and one sector has a capacity of 512 B. As described with reference to Fig. 13A, the logic cluster addresses are allocated into the memory space of 16 MB. As described with reference to Fig. 13B, the logical/physical address conversion table showing the correspondence relation between the logic cluster addresses and the physical cluster addresses is formed on a segment unit basis. Further, as mentioned above, the physical cluster addresses of 11 bits of A0, A1, ..., and A10 are used for the flash memory of 4 MB × 4 = 16 MB.

As shown in Fig. 2, the parallel writing can be performed to the flash memory 7. Fig. 2 shows only the portion regarding the data

input/output for simplicity of explanation. Four corresponding memory cells MC0 to MC3 are provided for storages 0 to 3, respectively. Data is supplied to the memory cells MC0 to MC3 through the data bus and flash buffers BF0 to BF3, respectively. That is, when the write data of one page is accumulated into each of the flash buffers BF0 to BF3 through the data bus, the data is simultaneously transferred from the flash buffers BF0 to BF3 to the memory cells MC0 to MC3. Although Fig. 2 shows an example in which one IC package has four storages, four flash memories of different packages can be also used. Further, a plurality of flash memories each having a plurality of storages in a package can be also combined.

Fig. 3 shows a more specific construction of the memory card 6 to which the invention can be applied. The memory card 6 is formed by constructing a control block 11 and the flash memory 7 as one chip IC. The bidirectional serial interface 5 between the CPU 1 of the data processing apparatus and the memory card 6 comprises ten lines. Four main lines are a clock line SCK for transmitting a clock upon data transmission, a status line SBS for transmitting a status, a data line DIO for transmitting data, and an interruption line INT. Two GND lines and two VCC lines are

provided as other power supplying lines. Two lines Reserv are undefined lines.

The clock line SCK is the line for transmitting the clock synchronized with the data. The status line SBS is the line for transmitting a signal indicative of the status of the memory card 6. The data line DIO is the line for inputting and outputting a command and enciphered audio data. The interruption line INT is the line for transmitting an interruption signal for requesting an interruption to the CPU 1 of the data processing apparatus from the memory card 6. The interruption signal is generated when the memory card 6 is attached. In the embodiment, however, since the interruption signal is transmitted through the data line DIO, the interruption line INT is connected to the ground and is not used.

A serial/parallel conversion, parallel/serial conversion, and interface cluster (abbreviated to an S/P, P/S, I/F cluster) 12 in the control block 11 is connected to the interface 5. The S/P, P/S, I/F block 12 converts the serial data received from the data processing apparatus into parallel data, fetches it into the control block 11, converts the parallel data from the control block 11 into the serial data, and sends it to the data processing apparatus.

In a format by which data is transmitted through the data line DIO, a command is first transmitted and, thereafter, data is transmitted. The S/P, P/S, I/F block 12 stores the command into a command register 13 and stores the data into a page buffer 14 and a write register 15. An error correction encoding circuit 16 is provided in association with the write register 15. The error correction encoding circuit 16 forms a redundancy code of an error correction code for the data temporarily stored in the page buffer 14.

The output data of the command register 13, page buffer 14, write register 15, and error correction encoding circuit 15 is supplied to a flash memory interface and sequencer (abbreviated to a memory I/F, sequencer) 17. The memory I/F, sequencer 17 is an interface between the control block 11 and flash memory 7 and controls the transmission and reception of the data between them. The data is written into the flash memory 7 through the memory I/F, sequencer 17.

The data read out from the flash memory 7 is supplied to the page buffer 14, a read register 18, and an error correcting circuit 19 through the memory I/F, sequencer 17. The data stored in the page buffer 14 is error corrected by the error correcting circuit 19. The error corrected outputs

of the page buffer 14 and read register 18 are supplied to the S/P, P/S, I/F block 12 and supplied to the CPU 1 of the data processing apparatus through the serial interface 5.

Reference numeral 20 denotes a configuration ROM in which version information, various attribute information, and the like of the memory card 6 have been stored. A switch 21 for prevention of erroneous erasure which can be operated by the user as necessary is provided for the memory card 6. When the switch 21 is in a connecting state of erasure inhibition, even if a command to instruct the erasure of the flash memory 7 is sent from the data processing apparatus side, the erasure of the flash memory 7 is inhibited. Further, reference numeral 22 denotes an oscillator for generating a clock serving as a reference for timing of the process of the memory card 6.

The serial interface between the data processing apparatus and memory card 6 in the embodiment of the invention will be described further in detail. When the data is read out from the memory card 6, a read command is transmitted to the memory card 6 from the data processing apparatus and the memory card 6 receives the read command. After completion of the transmission of the command, the memory card 6 executes a process for reading out

the data in the address designated by the received read command from the flash memory 7. While this process is being executed, a busy signal (high level) is transmitted to the data processing apparatus through the data line DIO. After completion of the reading of the data from the flash memory 7, the output of the busy signal is stopped and an output of a ready signal (low level) showing the completion of preparation for sending the data from the memory card 6 to the data processing apparatus is started.

By receiving the ready signal from the memory card 6, the data processing apparatus knows a fact that the process corresponding to the read command has been ready. The memory card 6 outputs the data read out to the page buffer to the data processing apparatus through the data line DIO. The status in which each of the above processes is executed is shown by a level change of the status line SBS.

When the data is written into the flash memory 7 of the memory card 6, a write command is transmitted from the data processing apparatus to the memory card 6 via the data line DIO. A write address is transmitted in association with the write command. Although the writing and reading operations of the data are performed on a sector

unit basis in the flash memory 7, the file is managed on a cluster unit basis in the data processing apparatus and addresses from the data processing apparatus are based on a cluster unit. Subsequently, the data processing apparatus transmits the write data to the memory card 6 through the data line DIO. In the memory card 6, the received write data is accumulated into the page buffer. When the transmission of the write data is finished, the memory card 6 executes a process for writing the write data into the flash memory 7. A busy signal is outputted during the writing process. When the writing process of the write data is finished in the memory card 6, the output of the busy signal is stopped and the ready signal (low level) is transmitted to the data processing apparatus.

In case of performing the parallel writing operation via the serial interface, a command, an address, and data for writing into the storage 0 are transmitted and, thereafter, in a state where the busy signal is at the high level, a command, an address, and data for writing into the storage 1, a command, an address, and data for writing into the storage 2, and a command, an address, and data for writing into the storage 3 are sequentially transmitted. The command, address, and data for

writing into the storage 0 are again transmitted. At this time point, the previous writing process of the data into the storage 0 has been finished and the busy signal is at the low level. The parallel writing can be performed by repeating such an operation. The commands, addresses, and data can be also simultaneously transmitted by a method of using four serial interfaces in parallel.

The above embodiment of the invention will be described further in detail. Fig. 4 shows a construction of the address in the embodiment. Address spaces in the memory are shown by 11 bits of A0, A1, …, and A10. A0 indicates the LSB (least significant bit) and A10 indicates the MSB (most significant bit). The storages each having a capacity of 4 MB are switched by the LSB (A00) and the second LSB (A1). The addresses of 9 bits of A2 to A10 are allocated to the sectors and segments in the respective storages.

Fig. 5 is a diagram for explaining a file managing method in the system of Fig. 1 using the memory card 6 as a storing medium. In Fig. 5, reference numeral 30 denotes data in a data file, for example, in a compressed audio data file. As for the compressed audio data, usually, a file is formed every music piece and the file is recorded into the flash memory 7 in the memory card 6 on a

sector unit basis and read out from the flash memory 7.

In case of recording such data 30 into the flash memory 7 in parallel, as shown in Fig. 5, writing sectors are selected from a plurality of clusters so that the sectors are continuously arranged in each cluster after the writing process and the data is simultaneously written into the selected sectors. Now, assuming that the size of data 30 coincides with four clusters, the data 30 is recorded into the four clusters in the flash memory 7.

As shown in Fig. 5, the data is recorded so that the sectors are arranged in each cluster in each storage in the original order after the writing. For example, in the case where the sectors numbered as 0, 1, 2, 3, ... in the original order are written into the storages 0 to 3 in parallel, the data of No. 0 is recorded into the head sector in the cluster in the storage 0, the data of No. 16 is recorded into the head sector in the cluster in the storage 1, the data of No. 32 is recorded into the head sector in the cluster in the storage 2, and the data of No. 48 is recorded into the head sector in the cluster in the storage 3, respectively.

As mentioned above, when the data is numbered every sector, four data units of the

numbers having offsets of the number which is equal to the number of sectors of the cluster are converted into parallel data and simultaneously written into four storages. Thus, in each storage in the flash memory 7, the data is arranged in the original order into the cluster constructed in the same storage in a manner similar to that of the existing flash memory. Therefore, the compatibility with the file format of the existing flash memory is held.

The data is sequentially read out every cluster from the flash memory recorded as mentioned above. For example, the data is sequentially read out from the head sector of the cluster in the storage 0 in Fig. 5. Subsequently, the data is sequentially read out from the head sector of the cluster in the storage 1. In this manner, the data is sequentially read out from the cluster in the storage 2 and the cluster in the storage 3. The order of the read-out data is the same as the original order. The erasing operation is performed on a cluster unit basis constructed every storage.

As mentioned above, according to the data arrangement after the parallel writing in the embodiment, the cluster is constructed in the same storage in a manner similar to the existing flash memory. Therefore, the compatibility of the file

format with that of the existing flash memory can be held.

Fig. 6 shows the writing operation in the embodiment. Data is first transferred from the host side to the page buffer of the sector size. Further, the data is transferred from the page buffer into the flash buffer BF0 of the storage 0. The time T is required to transfer. For the next write busy period, the data is written from the flash buffer BF0 into the storage 0. After the first transfer period T, the data of the next sector is transferred and written into the storage 1 for the write busy period. Since the writing operation into the storages 0 to 3 is performed in parallel as mentioned above, the writing speed higher than that in the conventional writing operation shown in Fig. 15 is accomplished.

Upon reading, as shown in Fig. 7, for a read busy period, the data is read out from each of the storages 0 to 3 and the read-out data is transferred to the flash buffers BF0 to BF3 of the sector size. At the next transfer time T, the data is transferred from the flash buffer BF0 to the page buffer and, further, the data is transferred from the page buffer to the host side. Subsequently, the data is sequentially outputted from the flash buffers BF1, BF2, and BF3 to the page buffers and

the data is transferred from the page buffers to the host side. The reading speed higher than that in the process of the conventional reading operation in which the read busy operations are sequentially performed (Fig. 16) is accomplished.

Fig. 8 is a flowchart showing a flow for processes in case of writing data into continuous logic sectors 0 to 3 belonging to the different clusters in a certain segment. In first step S1, a logical/physical conversion table is formed with respect to a segment as a target to be written. In step S2, sector 0 is sent from the host side to the page buffer and the data in sector 0 is transferred from the page buffer to the flash buffer. The time T is required to transfer. In next step S3, in parallel with the sending of sector 1, sector 0 is written into one storage in the flash memory in step S4.

In step S5, sector 2 is sent. In step S6, sector 1 is written into one storage in the flash memory in parallel. Subsequently, processes for sending of sector 3 (step S7), writing of sector 2 (step S8), and writing of sector 3 (step S9) are similarly performed. According to the embodiment of the invention, the situation such that the acceses are concentrated to one storage as in the conventional apparatus does not occur, and the

segments are not switched. Therefore, since there is no need to form the logical/physical conversion table, the high processing speed can be realized.

As an example of a storage switching method at the time of performing the parallel writing operation as mentioned above and reading out the written data will be described. Fig. 9 shows a construction for supplying addresses to four storages in the embodiment. Fig. 10 shows physical addresses in the flash memory of 4 MB × 4 = 16 MB.

As described with reference to Fig. 4, the physical addresses are expressed by 11 bits of A0, A1, …, and A10. A0 indicates the LSB (least significant bit) and A10 shows the MSB (most significant bit).

In the embodiment of the invention, when the formed addresses A0 to A10 of 11 bits are sent to the flash memory, the addresses A2 to A10 are supplied to the flash memory as addresses for specifying the addresses of the sectors and segments. Two lower bits of A0 and A1 are supplied to the flash memory as addresses for specifying the storage switching. That is, as shown in Fig. 9, the addresses A2 to A10 of nine bits on the upper side are sent in common to the four storages (0 to 3). The addresses A0 and A1 of two bits on the lower side are supplied to a 2-to-4 decoder 40. Selection

signals CS0, CS1, CS2, and CS3 for selecting each storage are generated from the decoder 40. When (A1, A0) = 00, the selection signal CS0 to select the storage 0 is generated from the decoder 40. When (A1, A0) = 01, (A1, A0) = 10, or (A1, A0) = 11, the selection signal CS1, CS2, or CS3 for selecting the storage 1, storage 2, or storage 3 is generated from the decoder 40, respectively. In the constructional example of Fig. 3, the decoder 40 is provided in the memory I/F, sequencer 17.

In case of performing the storage switching as mentioned above, an address change at the time when the physical address is increased from the address in which all 11 bits are equal to 0 to the address in which all 11 bits are equal to 1 is shown by arrows in Fig. 10. That is, the address change starts from the head cluster of the storage 0. Subsequently, the head cluster of the storage 1 is designated. When the address changes to the head cluster of the storage 3 via the head cluster of the storage 2, the physical cluster address changes so that the cluster is shifted to the second cluster of the storage 0.

Fig. 11 shows an arrangement of the segments and the logic cluster addresses in the embodiment of the invention. As will be understood from the arrangement of the logic cluster addresses

in Fig. 11, 512 clusters included in one segment are constructed by 128 clusters included in each of the four storages. The logical/physical address conversion table is formed every segment. Therefore, if no segment is changed, the logical/physical address conversion table to be referred to or updated is not changed, so that a deterioration of the reading performance due to the access to the table or the updating of the table can be prevented. The data can be simultaneously written into the continuous logic cluster addresses, for example, 0x0004 to 0x0007.

When the logic cluster addresses are discontinuous like 0x0000, 0x0200, 0x0400, and 0x0600, since those addresses exist in one storage, the data cannot be simultaneously written. However, since a probability that the process for writing the continuous logic sectors into such discontinuous cluster addresses actually occurs is very low, a large problem will not occur.

Although the embodiment has been described above with respect to the flash memory of 4 MB in which one sector consists of 512 B, one cluster consists of 8 kbytes, and one storage consists of 512 clusters, those values are shown as an example and the invention can be also applied to flash memories of other numerical values. For example,

the capacity of one cluster can be set to 16 kB. The invention can be also applied to a flash memory such that a capacity of one storage is equal to 8 MB (1024 clusters × 8 kB), 16 MB (1024 clusters × 16 kB), 32 MB (2048 clusters × 16 kB), 64 MB (4096 clusters × 16 kB), or the like.

According to the invention, when data existing over a plurality of clusters is written, the data can be simultaneously written, so that the high speed writing can be performed. When the data existing over a plurality of clusters is written or read out, if it exists in the same segment, the switching of the logical/physical address conversion table can be made unnecessary, so that a high accessing speed can be realized.

CLAIMS

1. A data processing system in which a non-volatile memory apparatus having a plurality of storages in which one cluster is constructed by a plurality of sectors and one segment is constructed by a plurality of clusters is detachable to/from a data processing apparatus, wherein

said data processing apparatus has

address designating means for designating an address of the cluster in which data is recorded,

said memory apparatus has

recording means for recording the data into the address designated by said address designating means, and

the data of said plurality of clusters in said one segment is distributed and arranged into said plurality of storages.

2. A data processing apparatus using a non-volatile memory apparatus, as a recording medium, having a plurality of storages in which one cluster is constructed by a plurality of sectors and one segment is constructed by a plurality of clusters, wherein

said data is written into said memory apparatus so that data of said plurality of clusters in said one segment is distributed and arranged into said plurality of storages.

3. A non-volatile memory apparatus which is detachable to/from a data processing apparatus and has a plurality of storages in which one cluster is constructed by a plurality of sectors and one segment is constructed by a plurality of clusters, wherein

data of said plurality of clusters in said one segment is distributed and arranged into said plurality of storages.

4. An apparatus according to claim 1, 2, or 3, wherein

an access is performed with reference to a logic cluster address/physical cluster address conversion table.

5. A memory apparatus according to claim 3, wherein

a signal to switch said plurality of storages is formed from one or a plurality of bits on the lower side of an address.

6. A data recording method of recording, in parallel, data in which one cluster is constructed by a plurality of sectors and which exists over a plurality of said plurality of clusters into a plurality of storages, comprising the steps of:

designating a cluster address and writing data into the designated cluster address; and

after completion of the parallel writing

process, distributing and arranging the data of said plurality of clusters in one segment into said plurality of storages.

ABSTRACT

512 clusters included in one segment are distributed into 128 clusters included in each of four storages. A logical/physical address conversion table is formed every segment. Therefore, unless the segment is changed, the logical/physical address conversion table to be referred to or updated does not change, so that a deterioration of the reading performance due to an access to the table or an updating of the table can be prevented. Data can be simultaneously written into continuous logic cluster addresses, for example, 0x0004 to 0x0007, and the high speed writing operation can be realized.

Fig. 1

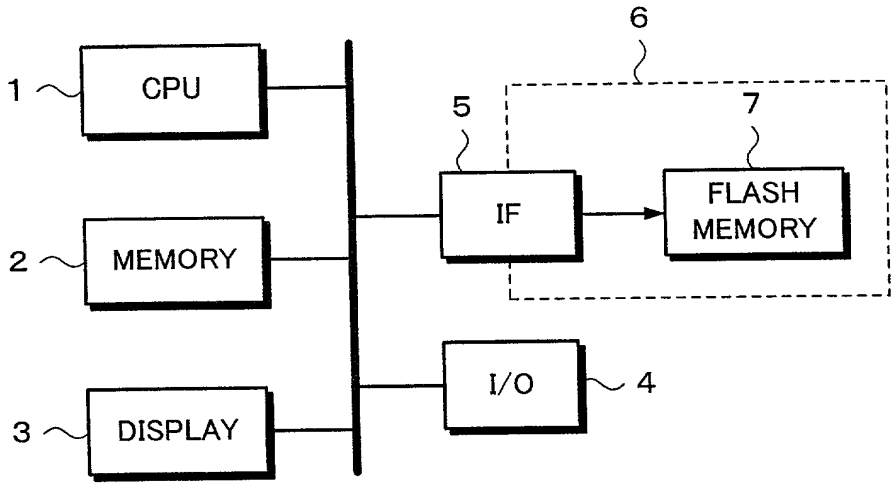

6
1
CPU
5
7
IF
FLASH MEMORY
2
MEMORY
I/O
4
3
DISPLAY

Fig. 2

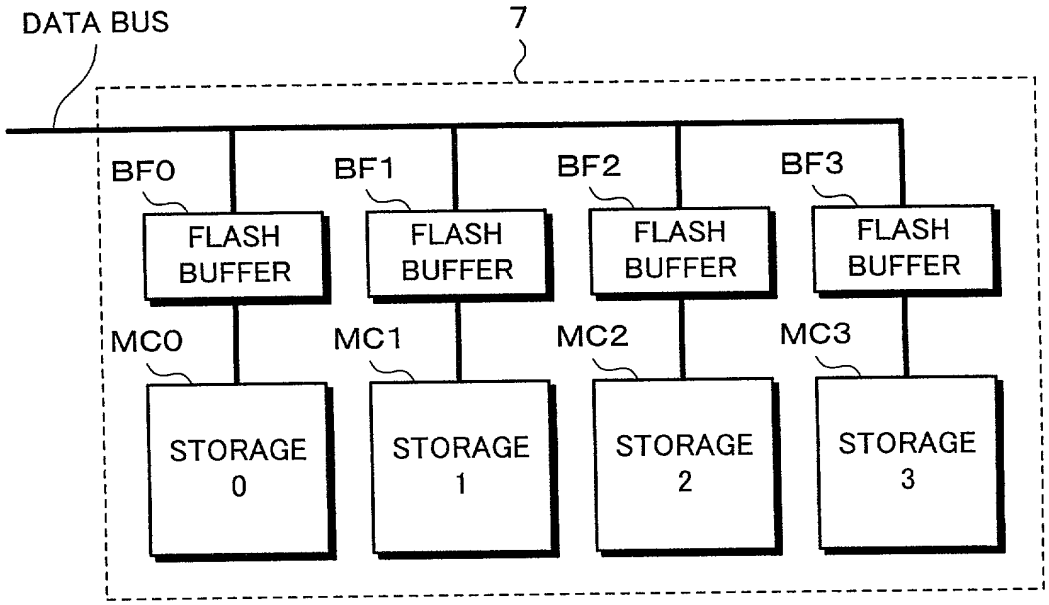

DATA BUS
7
BF0
BF1
BF2
BF3
FLASH BUFFER
FLASH BUFFER
FLASH BUFFER
FLASH BUFFER
MC0
MC1
MC2
MC3
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3

Fig. 3

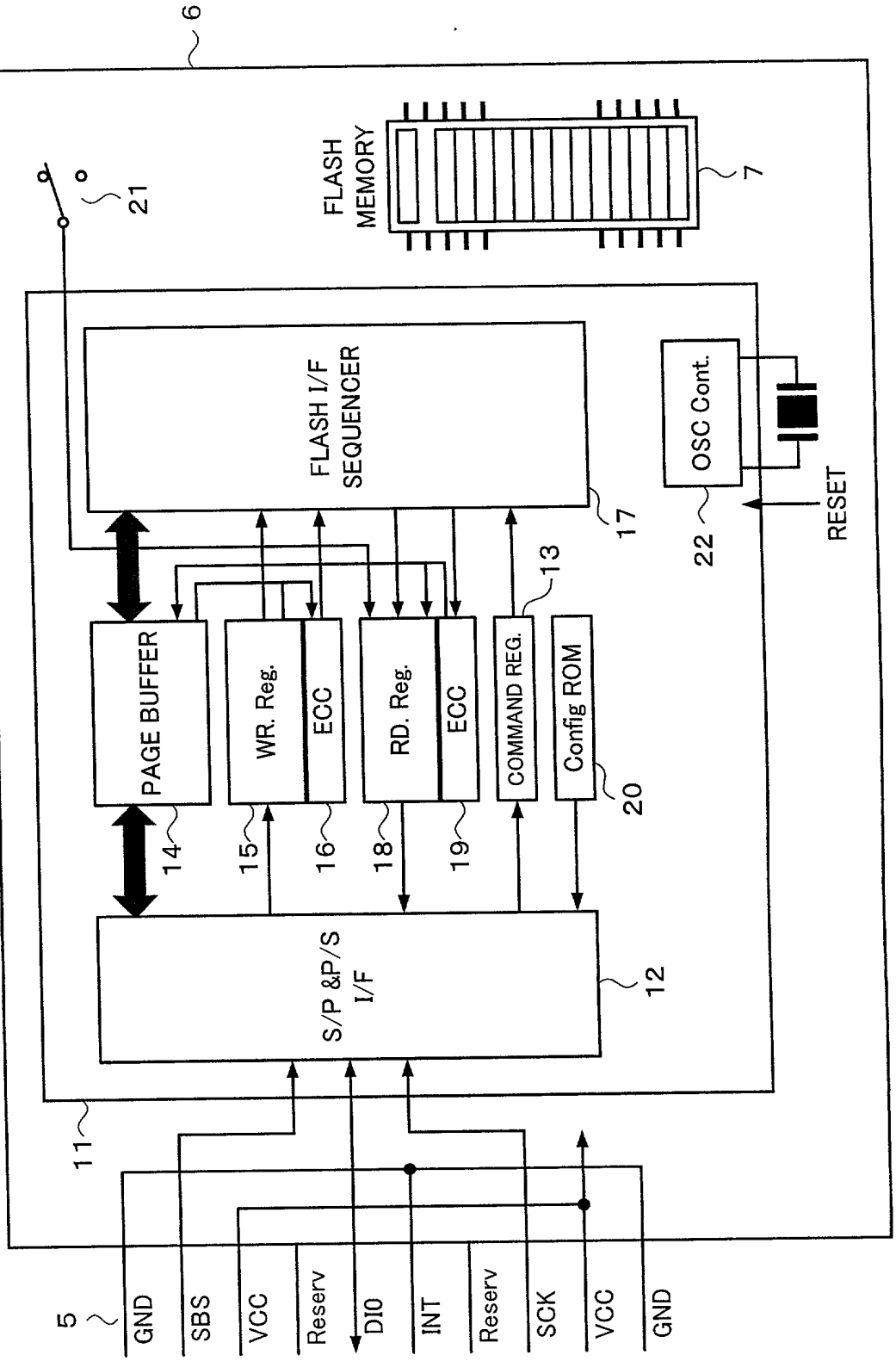

6
21
FLASH MEMORY
7
FLASH I/F SEQUENCER
17
OSC Cont.
22
RESET
PAGE BUFFER
14
WR. Reg.
15
ECC
16
RD. Reg.
18
ECC
19
COMMAND REG.
13
Config ROM
20
S/P &P/S I/F
12
11
5
GND
SBS
VCC
Reserv
DIO
INT
Reserv
SCK
VCC
GND

Fig. 4

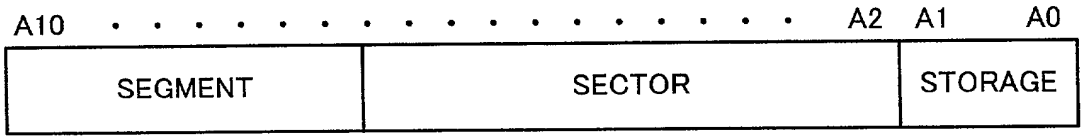

A10
A2
A1
A0
SEGMENT
SECTOR
STORAGE

Fig. 5

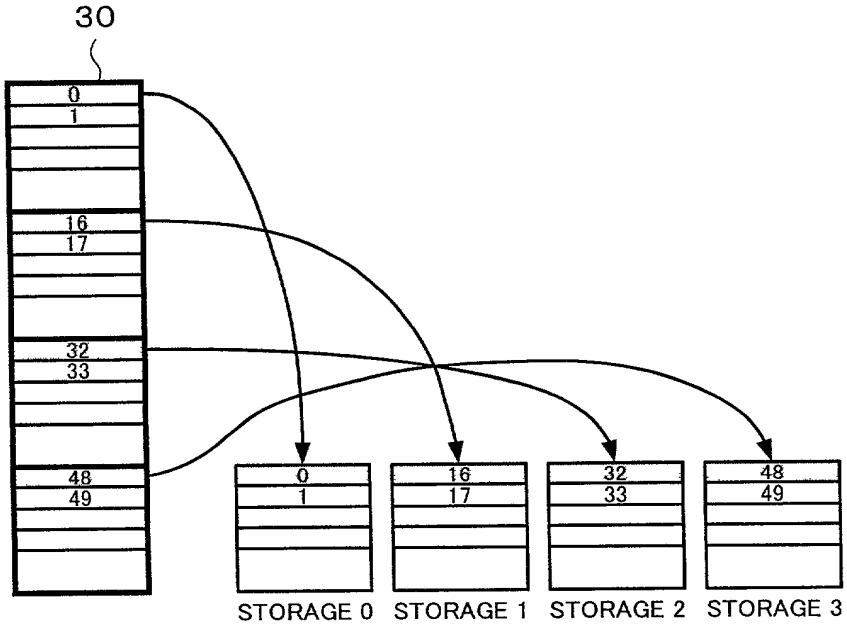

30
0
1
16
17
32
33
48
49
0
1
16
17
32
33
48
49
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3

Fig. 6

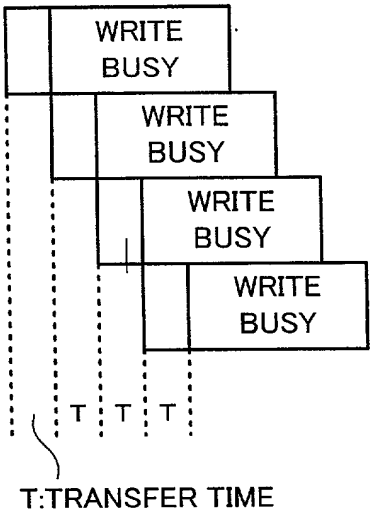

WRITE BUSY
WRITE BUSY
WRITE BUSY
WRITE BUSY
T
T
T
T:TRANSFER TIME

Fig. 7

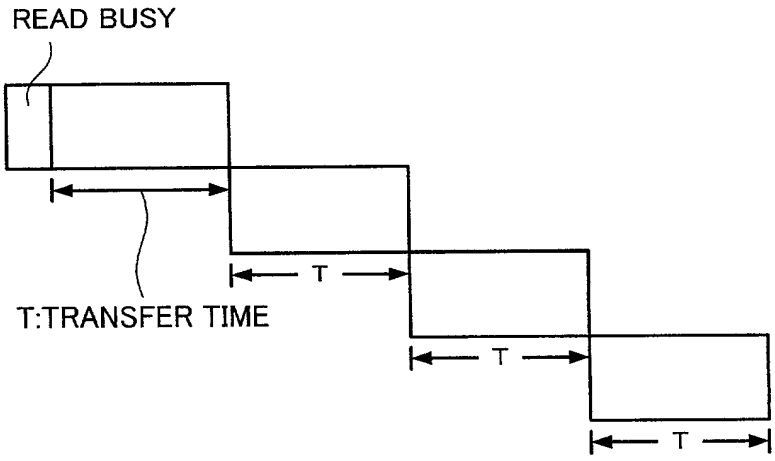

READ BUSY
T
T
T
T:TRANSFER TIME

Fig. 8

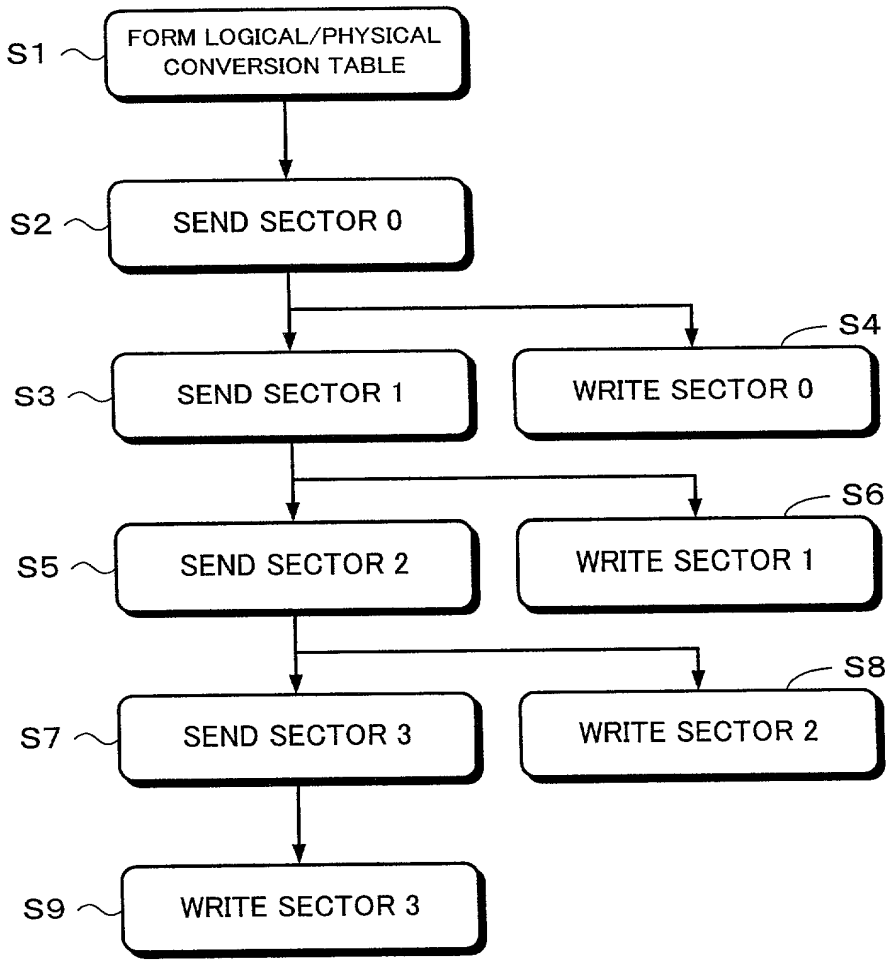

S1
FORM LOGICAL/PHYSICAL CONVERSION TABLE
S2
SEND SECTOR 0
S3
SEND SECTOR 1
S4
WRITE SECTOR 0
S5
SEND SECTOR 2
S6
WRITE SECTOR 1
S7
SEND SECTOR 3
S8
WRITE SECTOR 2
S9
WRITE SECTOR 3

Fig. 9

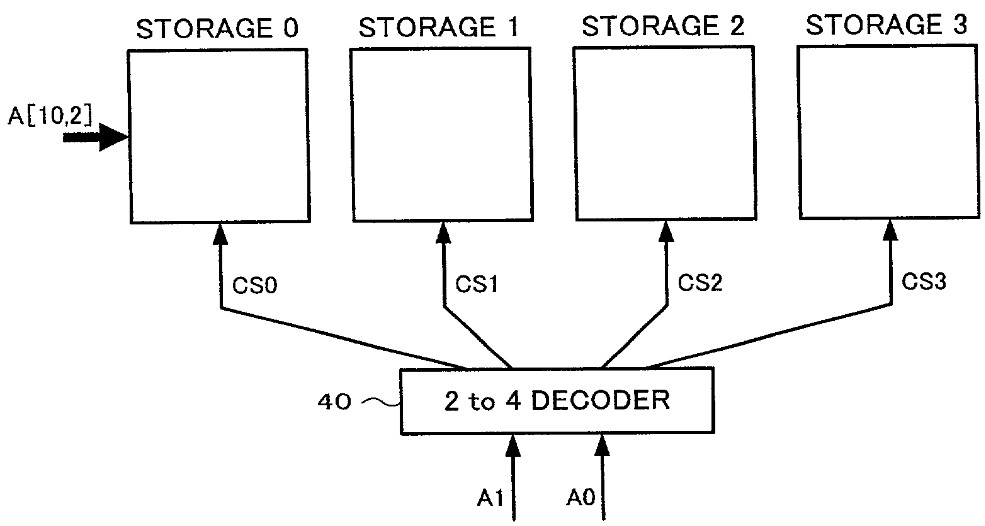


Fig. 10

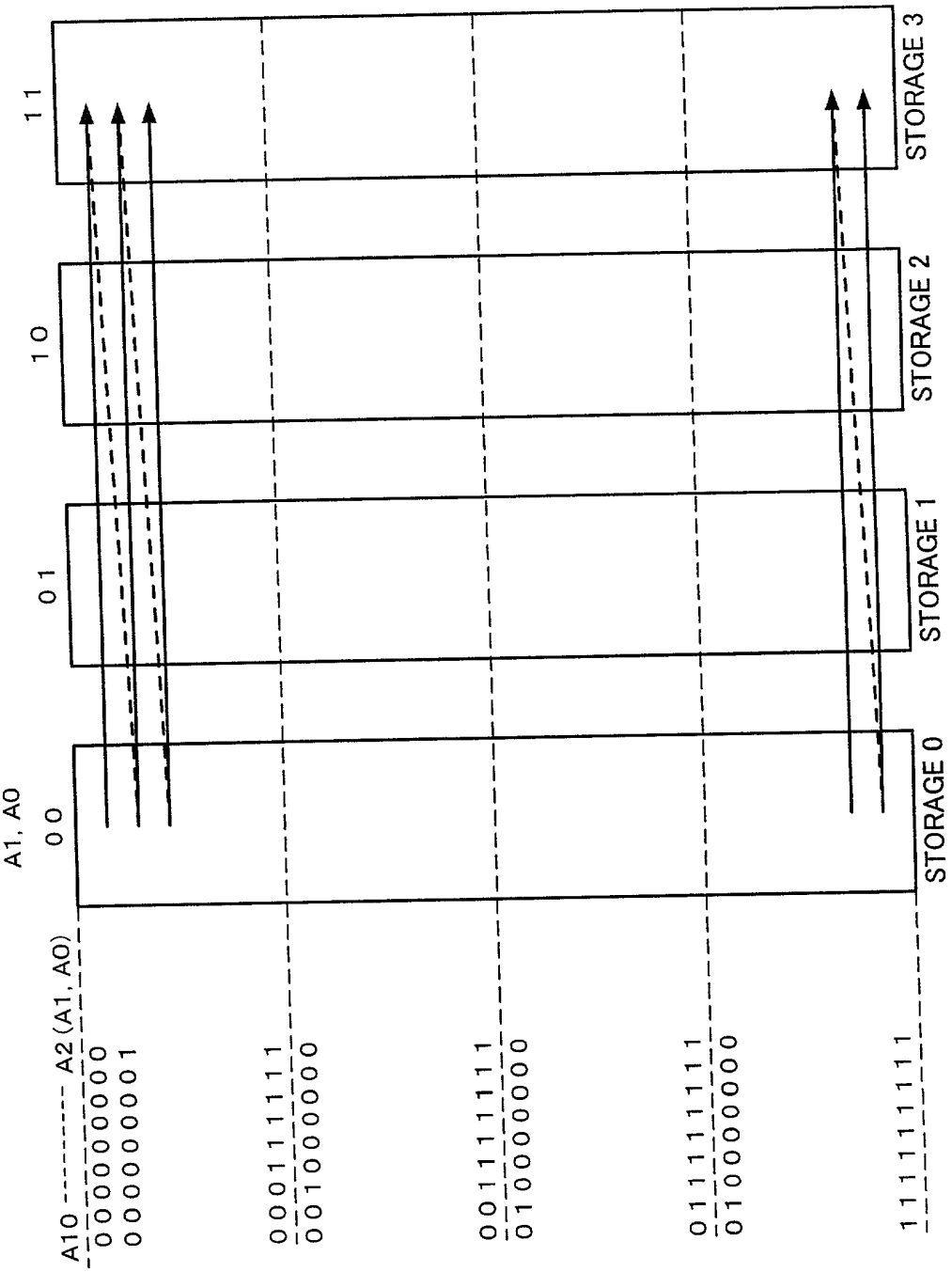

A1, A0
0 0
0 1
1 0
1 1
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
A10 ---------- A2 (A1, A0)
0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 1
0 0 0 1 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0 0
0 0 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1 1

Fig. 11

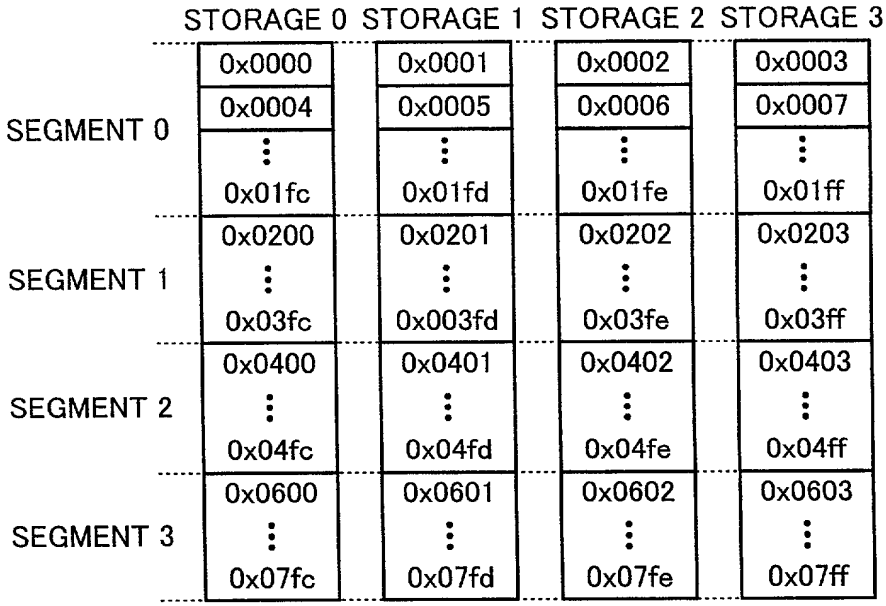

STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
SEGMENT 0
SEGMENT 1
SEGMENT 2
SEGMENT 3
0x0000
0x0001
0x0002
0x0003
0x0004
0x0005
0x0006
0x0007
0x01fc
0x01fd
0x01fe
0x01ff
0x0200
0x0201
0x0202
0x0203
0x03fc
0x003fd
0x03fe
0x03ff
0x0400
0x0401
0x0402
0x0403
0x04fc
0x04fd
0x04fe
0x04ff
0x0600
0x0601
0x0602
0x0603
0x07fc
0x07fd
0x07fe
0x07ff

Fig. 12

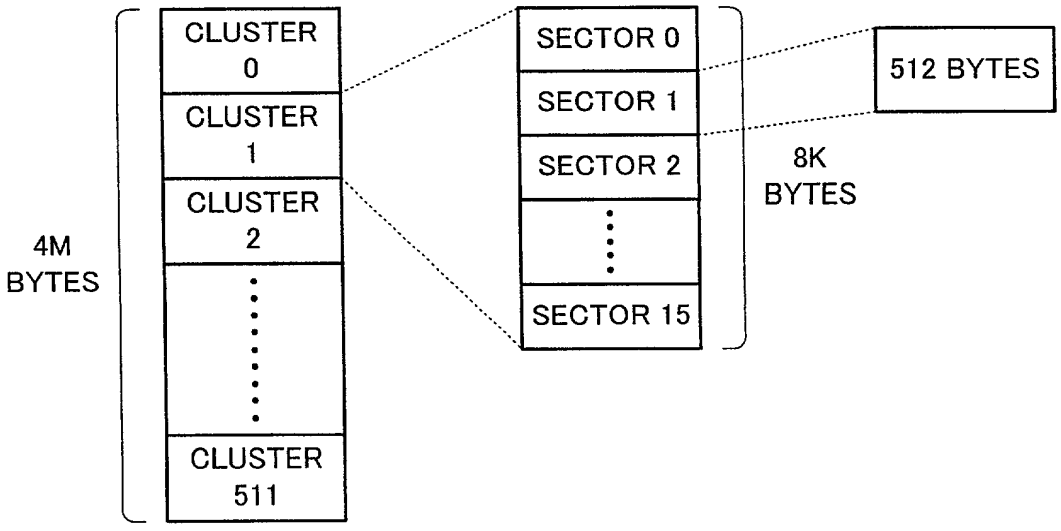

4M
BYTES
CLUSTER
0
CLUSTER
1
CLUSTER
2
CLUSTER
511
SECTOR 0
SECTOR 1
SECTOR 2
SECTOR 15
8K
BYTES
512 BYTES

Fig. 13A

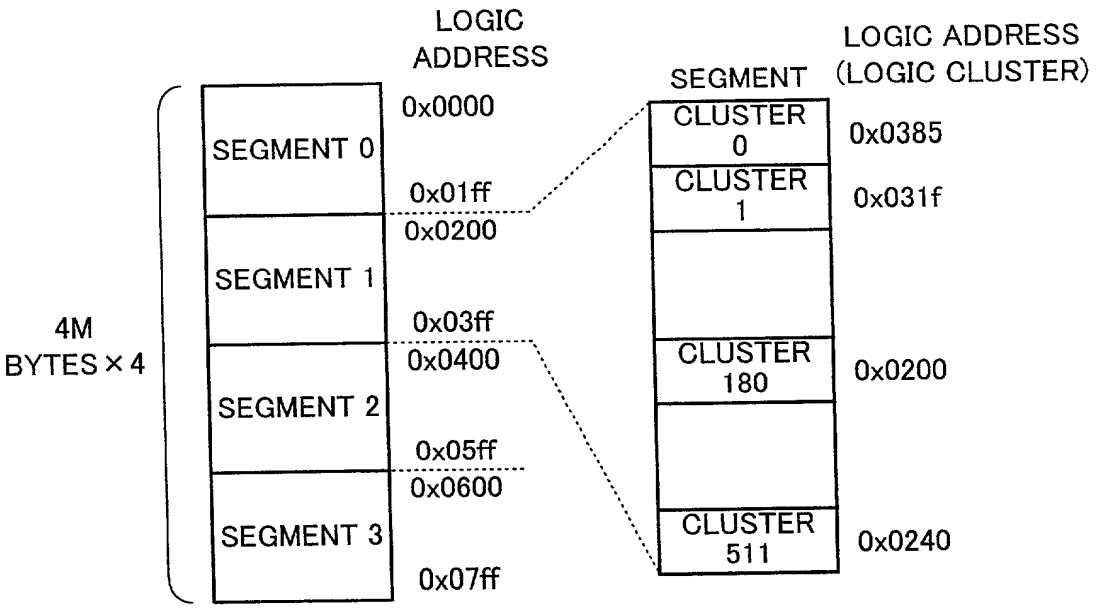


Fig. 13B

LOGIC ADDRESS	PHYSICAL ADDRESS
0x0200	180
0x0240	511
0x031f	1
0x0385	0

Fig. 14

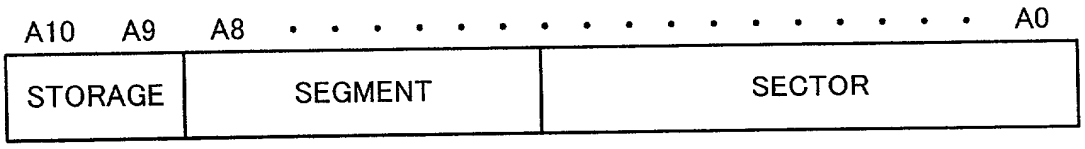


Fig. 15

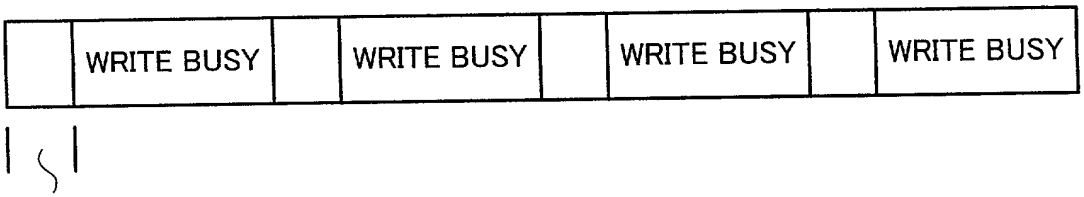


Fig. 16

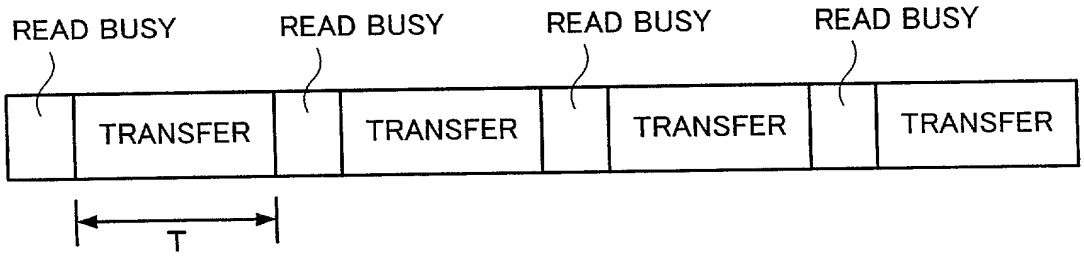


Fig. 17

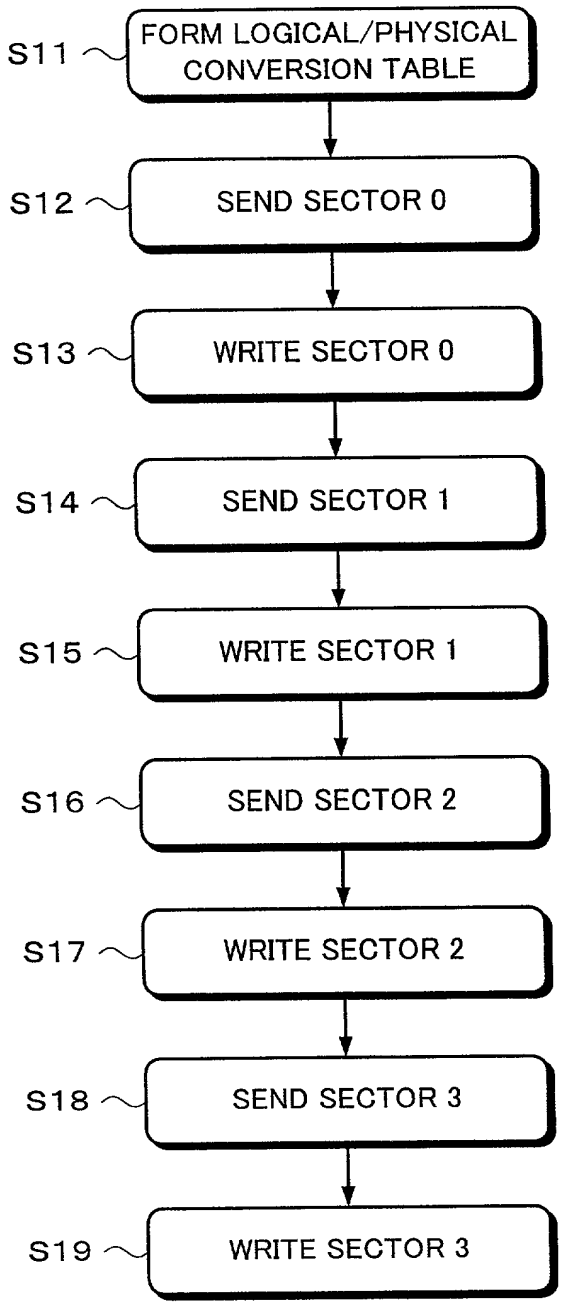

S11
FORM LOGICAL/PHYSICAL CONVERSION TABLE
S12
SEND SECTOR 0
S13
WRITE SECTOR 0
S14
SEND SECTOR 1
S15
WRITE SECTOR 1
S16
SEND SECTOR 2
S17
WRITE SECTOR 2
S18
SEND SECTOR 3
S19
WRITE SECTOR 3

Fig. 18

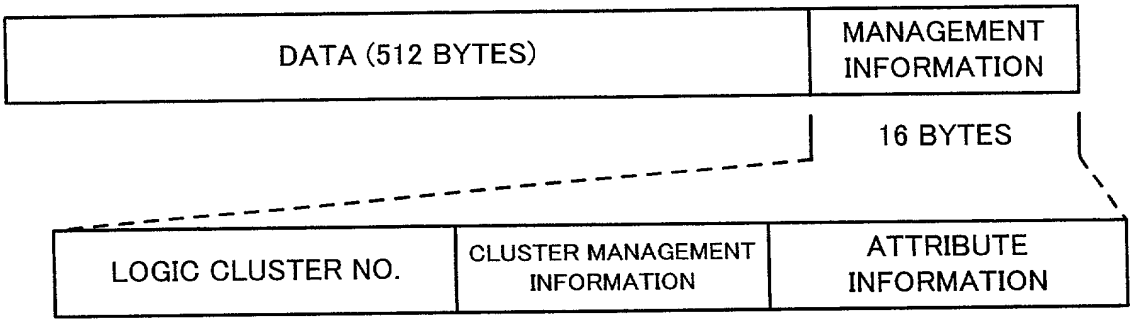

DATA (512 BYTES)
MANAGEMENT INFORMATION
16 BYTES
LOGIC CLUSTER NO.
CLUSTER MANAGEMENT INFORMATION
ATTRIBUTE INFORMATION

Fig. 19

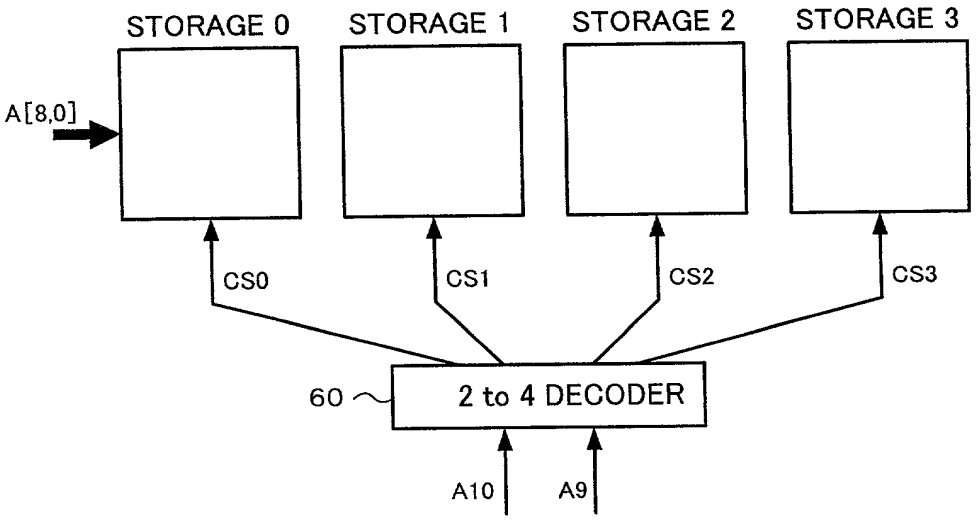

STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
A[8,0]
CS0
CS1
CS2
CS3
60
2 to 4 DECODER
A10
A9

Fig. 20

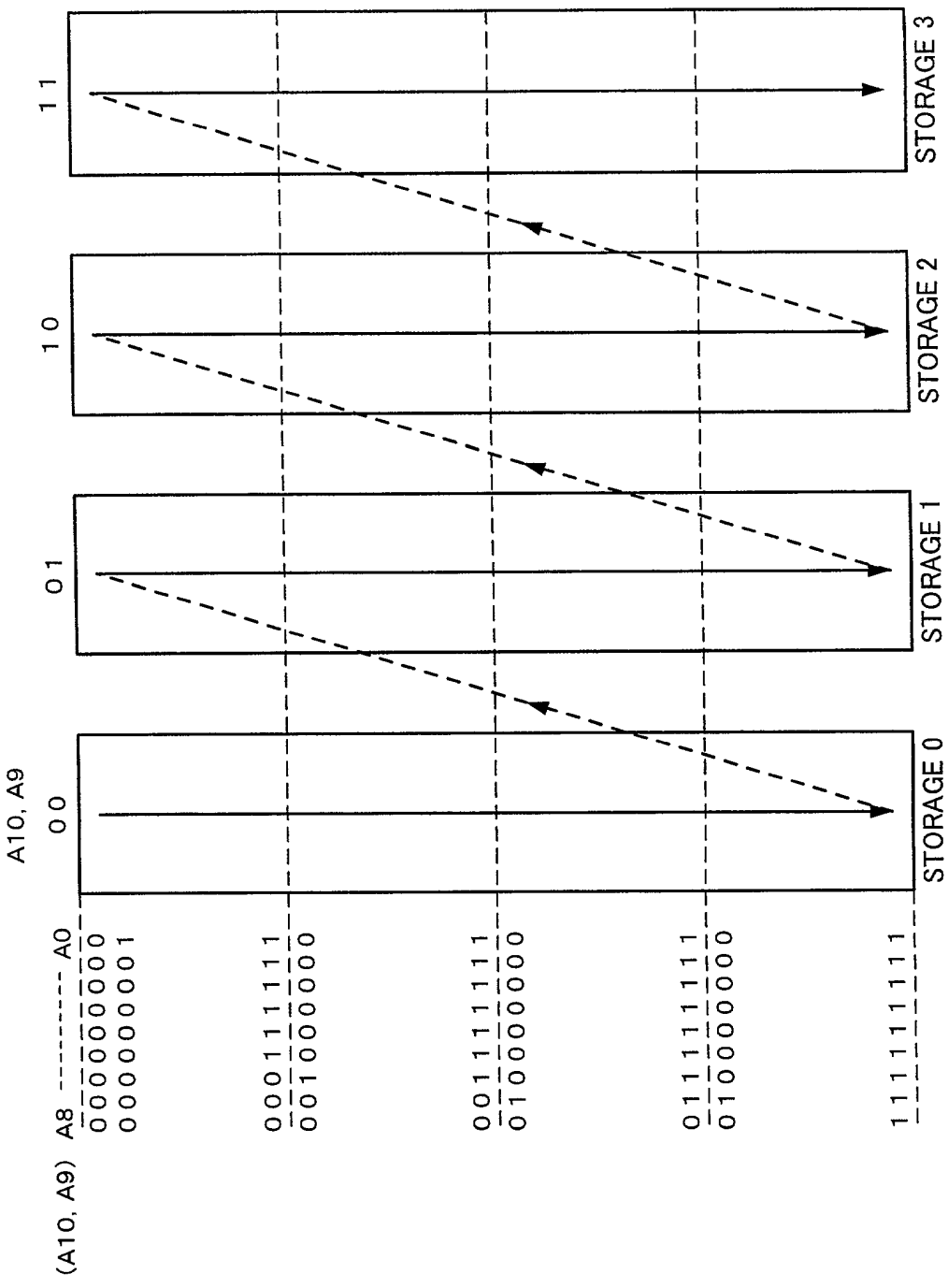
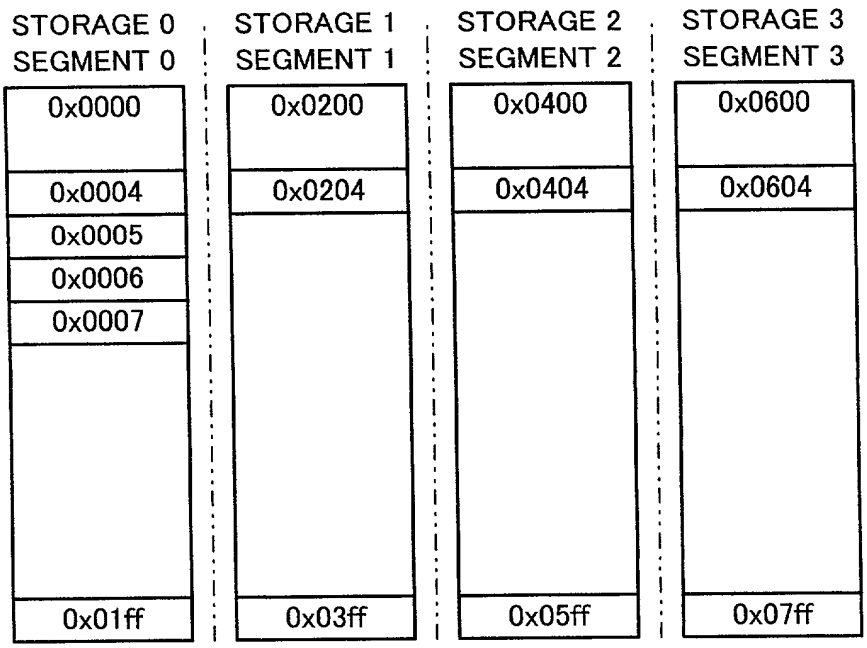

A10, A9
0 0
0 1
1 0
1 1
STORAGE 0
STORAGE 1
STORAGE 2
STORAGE 3
(A10, A9) A8 A0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 1
0 0 0 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0
0 0 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1

Fig. 21


STORAGE 0
SEGMENT 0
STORAGE 1
SEGMENT 1
STORAGE 2
SEGMENT 2
STORAGE 3
SEGMENT 3
0x0000
0x0004
0x0005
0x0006
0x0007
0x01ff
0x0200
0x0204
0x03ff
0x0400
0x0404
0x05ff
0x0600
0x0604
0x07ff

1.. CPU
5.. INTERFACE
6.. MEMORY CARD
7.. FLASH MEMORY

S00P0886 0500

PTO/SB 106 (5-00)
Approved for use through 10/31/02. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney for Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

私は、以下に記名された発明者として、ここに下記の通り宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先そして国籍は、私の氏名の後に記載された通りである。

My residence, post office address and citizenship are as stated next to my name:

下記の名称の発明について、特許請求範囲に記載され、且つ特許が求められている発明主題に関して、私は、最初、最先且つ唯一の発明者である（唯一の氏名が記載されている場合）か、或いは最初、最先且つ共同発明者である（複数の氏名が記載されている場合）と信じている。

I believe I am the original, first and sole inventor if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

RECORDING SYSTEM, DATA RECORDING APPARATUS, MEMORY APPARATUS, AND DATA RECORDING METHOD

上記発明の明細書はここに添付されているが、下記の欄がチェックされている場合は、この限りでない：

the specification of which is attached hereto unless the following box is checked:

☐ _____ の日に出願され、
この出願の米国出願番号またはＰＣＴ国際出願番号は、
_____ であり、且つ
_____ の日に補正された出願（該当する場合）

☒ was filed on 28 July 2000
as United States Application Number of
PCT International Application Number PCT/JP00/05055
_____ and was amended on
_____ (if applicable).

私は、上記の補正書によって補正された、特許請求範囲を含む上記明細書を検討し、且つ内容を理解していることをここに表明する。

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編規則１．５６に定義されている、特許性について重要な情報を開示する義務があることを認める。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

500P0886US00

Japanese Language Declaration

日本語宣言書

私は、ここに、以下に記載した外国での特許出願または発明者証の出願、或いは米国以外の少なくとも一国を指定している米国法典第３５編第３６５条(a)によるＰＣＴ国際出願について、同第１１９条(a)-(d)項又は第３６５条(b)項に基づいて優先権を主張するとともに、優先権を主張する本出願の出願日よりも前の出願日を有する外国での特許出願または発明者証の出願、或いはＰＣＴ国際出願については、いかなる出願も、下記の枠内をチェックすることにより示した。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT international application having a filing date before that of the application for which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
11-214089 (Number) （番号）		Japan (Country) （国名）	
	28 July 1999 (Day/Month/Year Filed)		☐
PCT/JP00/05055 (Number) （番号）		PCT (Country) （国名）	
	28 July 2000 (Day/Month/Year Filed)		☐
(Number) （番号）		(Country) （国名）	
	(Day/Month/Year Filed)		☐
(Number) （番号）		(Country) （国名）	
	(Day/Month/Year Filed)		☐
(Number) （番号）		(Country) （国名）	
	(Day/Month/Year Filed)		☐
(Number) （番号）		(Country) （国名）	
	(Day/Month/Year Filed)		☐

私は、ここに、下記のいかなる米国仮特許出願についても、その米国法典第３５編１１９条(e)項の利益を主張する。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) （出願番号）	(Filing Date) （出願日）

私は、ここに、下記のいかなる米国出願についても、その米国法典第３５編第１２０条に基づく利益を主張し、又米国を指定するいかなるＰＣＴ国際出願についても、その同第３６５条(c)に基づく利益を主張する。また、本出願の各特許請求の範囲の主題が、米国法典第３５編第１１２条第１段に規定された態様で、先行する米国出願又はＰＣＴ国際出願に開示されていない場合においては、その先行出願の出願日と本国内出願日またはＰＣＴ国際出願日との間の期間中に入手された情報で、連邦規則法典第３７編規則１．５６に定義された特許性に関わる重要な情報について開示義務があることを承認する。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365© of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in .Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) （出願番号）	(Filing Date) （出願日）	(Status: Patented, Pending, Abandoned) （現況：特許許可、係属中、放棄）

私は、ここに表明された私自身の知識に係わる陳述が真実であり、且つ情報と信ずることに基づく陳述が、真実であると信じられることを宣言し、さらに、故意に虚偽の陳述などを行った場合は、米国法典第１８編第１００１条に基づき、罰金または拘禁、若しくはその両方により処罰され、またそのような故意による虚偽の陳述は、本出願またはそれに対して発行されるいかなる特許も、その有効性に問題が生ずることを理解した上で陳述が行われたことを、ここに宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

S00P0886US00

日本語宣言書

委任状： 私は本出願を審査する手続を行い、且つ米国特許商標庁との全ての業務を遂行するために、記名された発明者として、下記の弁護士及び／または弁理士を任命する。（氏名及び整理番号を記載すること）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact al business in the Patent and Trademark Office connected therewith (list name and registration number)

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Full name of sole or first inventor

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(Supply similar information and signature for third and subsequent joint inventors)